

What is claimed is:

1. A bias circuit comprising:
  - an output node for outputting an output current;
  - an internal node;
- 5 a feedback amplifier comparing a first reference voltage with a voltage on the internal node and outputting a feedback signal;
- a current source controlled by the feedback signal;
- 10 a first differential transistor connected to the current source, the first differential transistor receiving a second reference voltage;
- a second differential transistor connected to the current source, the second differential transistor receiving the second reference voltage, the second differential transistor having a dimension that is different from that of the first differential transistor;
- 15 a first resistive transistor connected to the first differential transistor;
- a second resistive transistor connected to the second differential transistor, the second resistive transistor having a first gate;
- 20 a first mirror transistor having a second gate connected to the first gate, the first mirror transistor connected to the internal node; and
- 25 a second mirror transistor having a third gate connected to the first gate, the second mirror transistor connected to the output node.

2. A bias circuit according to claim 1, further comprising a resistor connected to the internal node.
3. A bias circuit according to claim 2, wherein the resistor is connected between the internal node and a 5 first potential source.
4. A bias circuit according to claim 2, wherein the resistor is an external resistor.
5. A bias circuit according to claim 1, wherein the first and second reference voltage are the same 10 voltage.
6. A bias circuit according to claim 1, further comprising a dummy differential transistor connected to the current source, the dummy differential transistor receiving the second reference voltage.
7. A bias circuit according to claim 1, wherein 15 the current source has a current source transistor having a gate connected to the feedback amplifier, a drain connected to the first and second differential transistor and a source connected to a first potential source.
8. A bias circuit according to claim 1, wherein 20 each of the first and second resistive transistors having a gate and a drain connected together and a source connected to a second potential source.
9. A bias circuit according to claim 1, wherein 25 each of the first and second mirror transistors having a source connected to a second potential source.
10. A bias circuit comprising:

an output node for outputting an output current;

an internal node;

a feedback amplifier comparing a first reference voltage with a voltage on the internal node and

5 outputting a feedback signal;

a current source controlled by the feedback signal;

a first differential transistor connected between the internal node and the current source, the first differential transistor receiving a second reference

10 voltage;

a second differential transistor connected to the current source, the second differential transistor receiving the second reference voltage, the second differential transistor having a dimension that is

15 different from that of the first differential transistor;

a first resistive element connected to the internal node;

a second resistive element connected to the second differential transistor; and

20 an output transistor having a gate connected to receive the feedback signal and a drain connected to the output node.

11. A bias circuit according to claim 10, wherein the output transistor has a source connected to a first

25 potential source.

12. A bias circuit according to claim 1, wherein the current source has a current source transistor having

a gate connected to the feedback amplifier, a drain connected to the first and second differential transistor and a source connected to a first potential source.

13. A bias circuit according to claim 1, wherein  
5 the first and second resistive elements are connected to a second potential source.

14. A bias circuit comprising:  
an output node outputting an output signal;  
an internal node on which an internal voltage is  
10 applied;

a feedback amplifier comparing a first reference voltage with the internal voltage;

a current source connected to a first potential source, the current source providing a constant current  
15 in response to the feedback signal;

a first differential transistor connected to the current source, the first differential transistor receiving a second reference voltage;

20 a second differential transistor connected to the current source, the second differential transistor receiving the second reference voltage, the second differential transistor having a dimension that is different from that of the first differential transistor;

25 a first resistive transistor connected between the first differential transistor and a second potential source;

a second resistive transistor connected between the

second differential transistor and the second potential source, the second resistive transistor having a first gate;

5 a first mirror transistor having a second gate connected to the first gate, the first mirror transistor connected between the internal node and the second potential source; and

10 a second mirror transistor having a third gate connected to the first gate, the second mirror transistor connected between the output node and the second power source.

15 15. A bias circuit according to claim 14, further comprising a resistor connected between the internal node and the first potential source.

16. A bias circuit according to claim 14, wherein the resistor is an external resistor.

17. A bias circuit according to claim 14, wherein the first and second reference voltage are the same voltage.

20 18. A bias circuit according to claim 14, further comprising a dummy differential transistor connected to the current source, the dummy differential transistor receiving the second reference voltage.

19. A bias circuit according to claim 1, wherein 25 the current source has a current source transistor having a gate connected to the feedback amplifier, a drain connected to the first and second differential

transistors and a source connected to the first potential source.

20. A bias circuit according to claim 14, wherein each of the first and second resistive transistors having 5 a gate and a drain connected together and a source connected to the second potential source.